ABSTRACT OF THE INVENTION

A power management system and circuit comprising instructions stored in computer memory for the prevention of simultaneous coupling of more than one power source to a device under test (DUT). An unpowered DUT residing on a pod is coupled to an in circuit emulator having a power grid which may be used to apply power to the DUT. Power for the DUT may also be applied directly to the DUT from a power source external to the in circuit emulator. Instructions stored in memory prevent the simultaneous application of power to the DUT from both the in circuit emulator power grid and an external power source. In the initial phase of testing, the Debug Software performs an acquire of the DUT to determine whether external power has been applied. External power applied to the DUT results in at least one activity signal detected by the computer, a bit is stored in the instruction set to prevent the application of in circuit emulator power and testing of the DUT continues under control of the Debug Software. In the absence of an activity signal from the DUT, the DUT is powered from the in circuit emulator power grid and detection of activity signals is continued. If no activity signal appears, the computer sets a bit in the instruction set that is interpreted as a fault condition in the DUT, and the Debug Software terminates testing. If an activity signal is detected by the computer, testing continues under control of the Debug Software.